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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,117	05/01/2006	Yuri Borisovich Sokolov	0155.0003US1	5024
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420 BEDFORD ST				
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EXAMINER				
BROCKMAN, ANGEL T				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary**Application No.**

10/578,117

Applicant(s)

SOKOLOV ET AL.

Examiner

ANGEL BROCKMAN

Art Unit

2463

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-11 is/are pending in the application.
- 5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-11 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 01 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-893)
Paper No(s)/Mail Date ____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Remarks, filed July 5, 2011 with respect to claims 1-11 have been fully considered and are persuasive. The 35 U.S.C. 103 (a) of claims 1-11 have been withdrawn.

Applicant argues Kato does not disclose how to determine when to send the polling signal. Examiner respectfully disagrees with the applicant. Kato discloses when to send the polling signal (column 6, lines 33-40, wherein the polling detect circuit and the timer, measures a period for responding (transmitting), column 7, lines 58-65, wherein the polling signal is the timing signal).

Claim Rejections - 35 USC § 103

1. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1,2, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. (US 6,021, 137, hereinafter Kato) and Findikli.(US 2002/0136198, hereinafter Findikli) in view of De Vul (US 3,479,628, hereinafter De Vul).

Regarding **claim 1**, Kato discloses a timing signal source periodically transmitting timing signals comprising one or more timing signal symbols and using a reference signal to determine when each timing signal is transmitted(column 6, lines 33-40, wherein the polling detect circuit and the timer, measures a period for responding (transmitting), column 7, lines 58-65, wherein the polling signal is the timing signal);a plurality of numbered slave units (figure 1, wherein slave units are terminals 2-4, column 10, lines 1-25); each numbered slave unit transmitting a data signal using its number and time when a timing signal is received to determine when to begin transmitting so that data signals from the slave units do not overlap with each other or with the timing signals (column 8, lines 14-30, wherein response signal is transmitted after a predetermined time to avoid overlap); a main unit receiving the data signals from the slave units ((130), wherein the data collector is the main unit). Kato does not disclose the superimposed signal includes AC current on a power line to determine when each timing symbol is received.

However, it is well known in the art that the AC power line includes a superimposed AC current (column 1, lines 25-36, column 3, lines 10-25). Kato does not disclose the slave units determine when each time symbol is received or a phase coded timing signal and generating time markers. Findikli discloses each numbered slave unit receiving at least one timing signal and using the voltage to determine when each timing signal symbol is received ([0026], [0031]); the slave units determine when each time symbol is received ([0031]). Findikli does not disclose phase coded timing signal. De Vault discloses a phase coded timing signal (column 2, lines 55-59) and generating time markers (column 4, lines 38-50). Thus, it would have been obvious to one of ordinary skill in the art to utilize the phase coded signal as disclosed by De Vault along with the system as disclosed by Findikli along with the data collection system as disclosed by Kato. Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the slave determination as disclosed by Findikli along with the system of Kato. The phase coded signal as disclosed by De Vault can be implemented in the system of Kato through software and hardware manipulation. The slave time reception determination as disclosed by Findikli can be implemented into the system of Kato through software implementation. The motivation for utilizing the phase coded signal as disclosed by De Vault along with the system as disclosed by Findikli and Kato. The motivation for utilizing the phase coded signal and time marker as disclosed by De Vault along with the system as disclosed by Findikli and Kato is to increase the efficiency of the timing between master and slave devices (column 1, lines 30-45). The motivation for utilizing the slave reception determination as disclosed by Findikli along with the system of Kato is to increase efficiency of the network and to synchronize the pulse from the master device (column 2, lines 35-40, Findikli)

Regarding **claim 2**, Kato discloses in case of temporary absence of the timing signals, the slave units continue transmission computing when to begin transmitting using a previously received timing signal (see figure 6, figure 7, column 9, lines 54-66, where the period of time waited is the absence of timing signal and the polling signal is low response signal of A1 includes the computing of the half-cycle).

Regarding **claim 6**, Kato discloses the timing signal source is the main unit (column 7, lines 58-65, wherein the data collector generates the timing signals).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato (US 6,021,137, hereinafter Kato), Findikli, and De Vault (US 3,479,628, hereinafter De Vault) in view of Tanaka et al.(US 4,998,245, hereinafter Tanaka).

Regarding **claim 4**, Kato discloses a timing signal is subjected to modulation (figure 8, where the reference signal is subjected to the primary modulating circuit. Kato, Findikli, and De Vault disclose all subject matter of the claimed invention with the exception of broadcast data transmission from a main unit to slave ones. Tanaka discloses broadcast data transmission from a main unit to slave ones (figure 1, figure 5, column 3, lines 15-40). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the broadcast transmission of Tanaka and modulation of Kato, Findikli, and De Vault. The modulation and broadcast transmission as disclosed by Tanaka can be implemented into the system of Kato, Findikli, and De Vault through software implementation. The motivation for utilizing the

modulation and broadcast transmission as disclosed by Tanaka in the system as disclosed by Kato, Findikli, and De Vaulis to increase the efficiency of the system.

5. Claims 3,5, and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over and Kato(US 6,021,137, hereinafter Kato), Findikli and De Vaul (US 3,479,628, hereinafter De Vaul). in view of (Lester et al.(US 6,784,790 B1, hereinafter Lester) .

Regarding **claim 3**, Kato, Findikli , and De Vauldisclose all subject matter of the claimed invention with the exception of source supplying a timing signal is not a system main unit but some other individual device. Lester discloses a source supplying a timing signal is not a system main unit (column 4, lines 61-67, column 5, lines 10-15, column 8, lines 20-47, where the IC is a micro chip or microprocessor). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the timing signal as disclosed by Lester along with the system as disclosed by Kato, Findikli, and De Vaul. The other units as disclosed by Lester can be implemented into the system as disclosed by Kato, Findikli, and De Vaulcan be manipulated through software. The motivation for utilizing another device as the timing signal as disclosed by Lester along with the system as disclosed by Kato, Findikli, and De Vaulis to increase the efficiency of the network.

Regarding **claim 5**, Kato discloses all signals being transmitted by a main and slave units have duration equal to 1/3 of the network voltage (column 14,lines 4-10, where the certain period of time is 1/3 of the network voltage). Kato, Findikli, and De Vauldisclose all subject matter of the claimed invention as set forth above in claim 1, with the exception of the zero crossing points centering. Lester discloses sending a timing signal of a predetermined form (figure 4A,

column 5, lines 53-66, column 6, lines 1-29, where the reference pulse includes the timing signal); zero crossing points of the fundamental harmonic of system supply network voltage (column 5, lines 55-65). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the duration of the network voltage and AC reference signal as disclosed by Kato, Findikli, and De Vaulalong with the system as disclosed by and Lester. The duration of the transmitted signals can be implemented using software. The motivation for utilizing the duration of 1/3 of the AC current voltage half-cycle and centered about zero crossing points is to increase the efficiency of the system.

Regarding **claim 7**, Kato, Findikli, and De Vauldisclose all subject matter of the claimed invention with the exception of each timing symbol is transmitted over a half-cycle of the AC current voltage. Lester discloses of each timing symbol is transmitted over a half-cycle of the AC current voltage(column 5, lines 43-65). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the half-cycling as disclosed by Lester along with the system as disclosed by Kato, Findikli, and De Vaul. The half-cycling can be implemented through software implementation. The motivation for utilizing the half-cycling is to increase the efficiency of the system.

Regarding **claim 8**, Kato, Findikli, and De Vauldisclose all subject matter of the claimed invention with the exption of the start of each timing signal symbol transmission is when the AC current voltage value is zero. Lester discloses the start of each timing signal symbol transmission is when the AC current voltage value is zero (column 2, lines 15-26, wherein the zero crossing

points mark beginning of transmission). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the zero crossings for transmission as disclosed by Lester along with the system as disclosed by Kato, Findikli, and De Vault. The zero crossings for transmission can be implemented through software implementation. The motivation for utilizing the zero crossings for transmission is to increase the efficiency of the system.

Regarding **claim 9**, Kato, Findikli, and De Vault disclose all subject matter of the claimed invention with the exception of each data signal is transmitted over a half-cycle of the AC current voltage. Lester discloses of each timing symbol is transmitted over a half-cycle of the AC current voltage (column 5, lines 43-65, therefore data is transmitted in the other half cycle, as a period is made up of one cycle). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the half-cycling as disclosed by Lester along with the system as disclosed by Kato, Findikli, and De Vault. The half-cycling can be implemented through software implementation. The motivation for utilizing the half-cycling is to increase the efficiency of the system.

Regarding **claim 10**, Kato, Findikli, and De Vault disclose all subject matter of the claimed invention with the exception of the start of each data signal transmission is when the AC current voltage value is zero. Lester discloses the start of each data signal symbol transmission is when the AC current voltage value is zero (column 2, lines 15-26, wherein the zero crossing points mark beginning of transmission). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the zero crossings for transmission as disclosed by Lester along with the system as disclosed by Kato, Findikli, and De Vault. The zero crossings

for transmission can be implemented through software implementation. The motivation for utilizing the zero crossings for transmission is to increase the efficiency of the system.

Regarding **claim 11**, Kato, Findikli, and De Vault disclose all subject matter of the claimed invention with the exception of an N-th half cycle of the AC current voltage (column 5, lines 43-65, therefore data is transmitted in the second or (N-th) half cycle, as a period is made up of one cycle). Thus, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize the half-cycling as disclosed by Lester along with the system as disclosed by Kato, Findikli, and De Vault. The half-cycling can be implemented through software implementation. The motivation for utilizing the half-cycling is to increase the efficiency of the system.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANGEL BROCKMAN whose telephone number is (571)270-5664. The examiner can normally be reached on Monday-Friday, 7:30-5:00pm.
7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick Ferris can be reached on 571-272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR

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system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANGEL BROCKMAN

Examiner

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/A. B./

Examiner, Art Unit 2463

/Derrick W Ferris/

Supervisory Patent Examiner, Art Unit 2463